**DSD Final Check Scores**

**1. Baseline**

(1) Area: (um2)

截圖:

(2) Total Simulation Time of given noHazard testbench: (ns)

截圖:

(3) Total Simulation Time of given hasHazard testbench: (ns)

截圖:

(4) Clock cycle for post-syn simulation (cycle in testbench, not cycle in sdc): (ns)